

REMARKS

Applicants gratefully acknowledge the Examiner's indication that claims 1-10, 15-17, and 25-27 are directed to allowable subject matter.

However, Applicants respectfully traverse the rejection of claims 11-14 and 18-24 as follows.

With regard to the rejection of claims 13, 18-19, and 22-24 as being anticipated by O'Brien (USP 6,886,110), note that Figures 3 and 5 of O'Brien are merely directed to various aspects of conventional boundary scan architecture. As seen in Figure 5, the boundary scan chain between the TDI and TDO pins of a particular device 30 can only contain the boundary scan registers within that device 30. O'Brien has no structure for forming a boundary scan chain between a device's TDI and TDO pins that also includes boundary scan registers 44 from another device such as a second device 30. Note that TDI pin 64 and TDO pin 66, to which the Examiner refers, are on different devices.

In sharp contrast, claim 13 is directed to a device (such as device 10 in application Figure 1) that includes "a second plurality of boundary scan cells" (such as cells 205 in Figure 2a) as well as a TDI pin and a TDO pin. At least one external device (such as device 20 in Figure 2b) includes a first plurality of boundary scan cells (such as shown within device 20). The claimed device also includes a means for forming a primary boundary scan chain (such as scan chain 200 in Figure 2a) between the TDI pin and the TDO pin including only the second plurality of boundary scan cells and for forming a secondary boundary scan chain (such as scan chain 230 in Figure 2b) between the TDI pin and the TDO pin including the first and the second plurality of boundary scan cells. In the claimed device, as opposed to the disclosure of O'Brien, the TDI pin and TDO pin that define the scan chain are on the same device whether the scan chain that is formed contains only the second plurality of boundary scan cells or both

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the first and second pluralities. Accordingly, claim 13 and its dependent claims 14 – 17 are allowable over O'Brien.

Claim 18 and its dependent claims 19-24 are also patentable over O'Brien. For example, claim 18 requires the claimed semiconductor device to include "a plurality of scan cells forming a scan chain" as well as a "first data input pin adapted to receive configuration and/or test data" and "first and second data output pins adapted to transmit configuration and/or test data." The semiconductor device is configurable to "couple the scan chain between the data input pin and the first data output pin in a first configuration" and "to couple the scan chain between the data input pin and the second data output pin in a second configuration." But as seen in Figures 3 and 5 of O'Brien, a conventional boundary scan device 30 includes just a single data input pin (TDI) 64 and a single data output pin (TDO) (unlabeled but referred to as 62 by the Examiner) for its scan chain. However, TDO pin 66, which the Examiner suggests is a second data output pin within the meaning of claim 18, is not included in device 30. Rather pin 66 is included in a separate device 30" and thus does not meet the requirements of claim 18. Accordingly, claims 18 – 24 are patentable over O'Brien.

With regard to the obviousness rejection of claims 14 and 20-21 as being unpatentable over O'Brien in view of an Official Notice that "using a state of a configuration memory cell for controlling [a] circuit is well known in the art" and that "a programmable logic device or a programmable power supply sequence controller is well known in the art, such notices do nothing to cure the infirmities of O'Brien as described above.

Applicants traverse the rejection of claims 11 -12 as being obvious over O'Brien (USP 6,886,110) in view of Crouch (USP 5,592,493) for analogous reasons as set forth with regard to claim 13. For example, claim 11 includes the act of "configuring the demultiplexer into a first configuration to couple the output of the shift register to the TDO pin such that a primary

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boundary scan chain is formed in just the first plurality of boundary scan cells" that is neither taught nor suggested by the O'Brien reference. The Crouch reference adds nothing further. In particular, note that Crouch's Figure 2 is simply an implementation of the scan architecture shown in Figure 1. As seen in Figure 1, Crouch provides a plurality of individual scan chains corresponding to the plurality of "functional blocks" (elements 12-22). The test controller 10 selects for a particular block's scan chain. The selected scan chain then flows through mux 24 and out through the output pin(s) STDO. But Crouch in no way enables or suggests the provision of a first scan chain that includes only a single device's cells and also the provision of a second scan chain that includes the single device's cells as well as the cells of external devices. Accordingly, claims 11-12 are patentable over the combination of the O'Brien and Crouch references.

In addition, the specification has been amended to address some minor typographical errors and to provide a U.S. Pat No. corresponding to a previously-stated U.S. Application No.

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For at least the above reasons, applicants submit that the claims are in condition for allowance and such action is respectfully requested.

If there are any questions regarding any aspect of the application, please call the undersigned at (949) 752-7040.

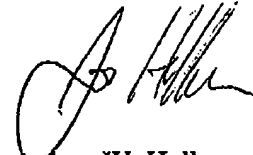
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